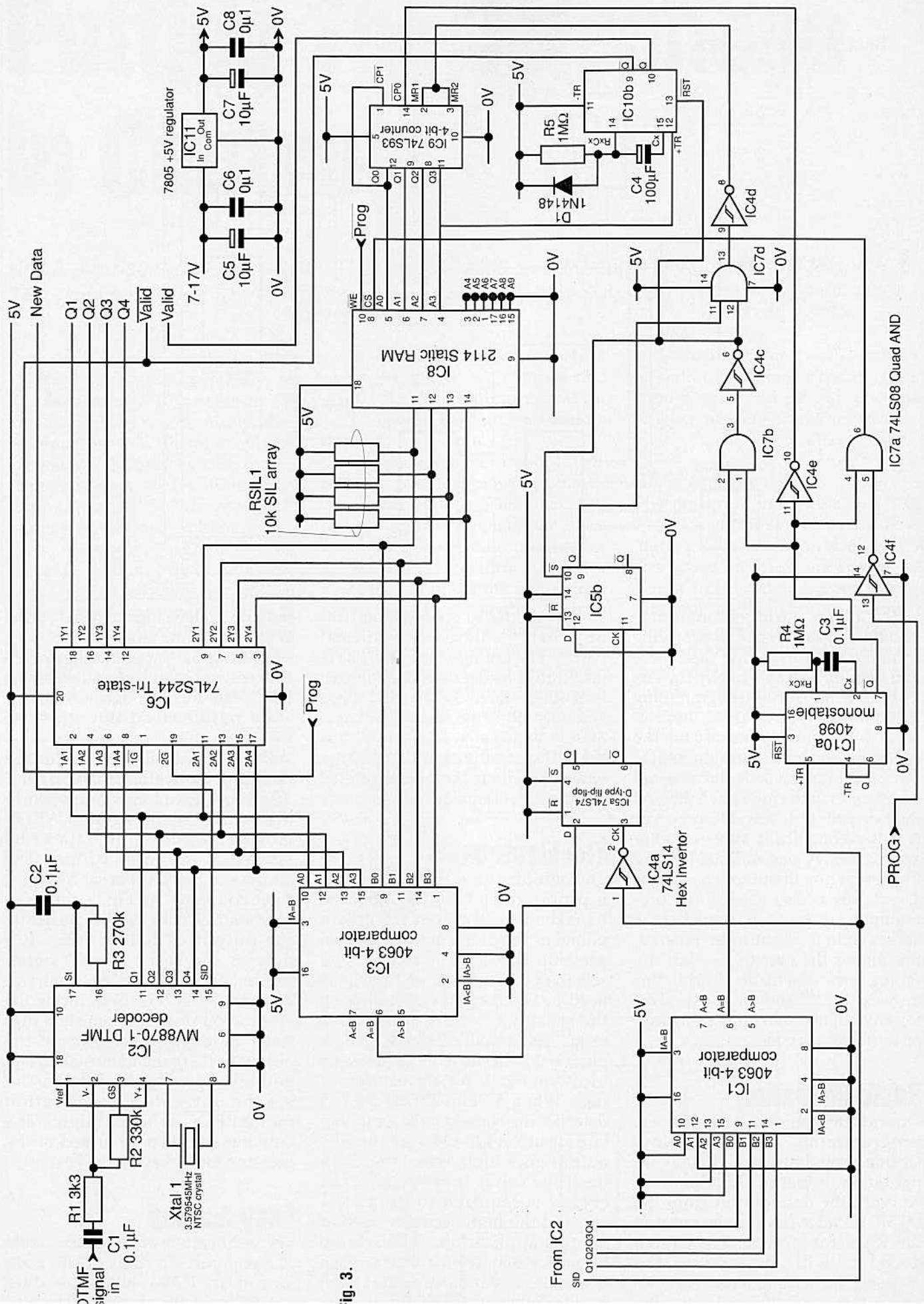


Fig. 3.

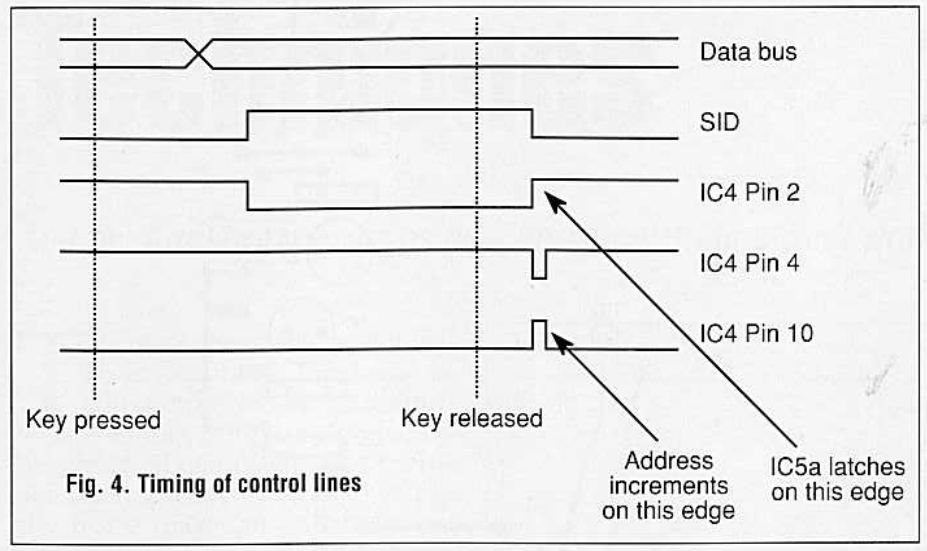


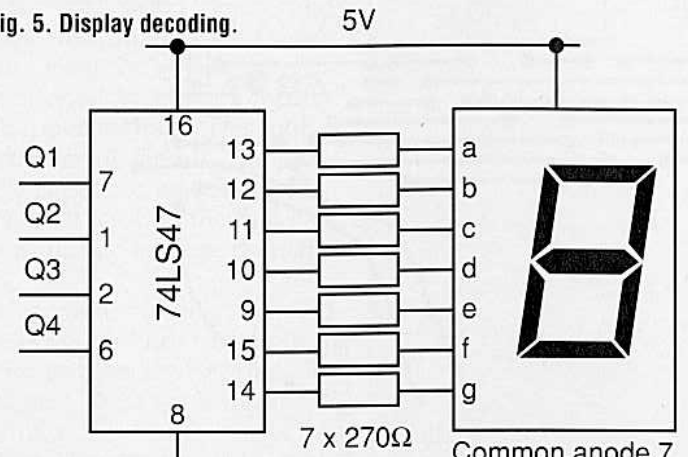
Fig. 4. Timing of control lines

put of IC3 is latched by IC5a when the key is released. When a difference in the two digits is detected the $\overline{Q}$ output of IC5(a) will go high, causing a low to be latched into IC5(b). The low at IC5(b)'s output will then reset the address counter for the RAM and so the VALID output will be prevented from going high. The output of IC5(b) must be SET high again which is done by pressing the '*' key – this should make it more difficult for anybody to 'stumble' across the correct code.

Fig 4 shows the sequence of data on the control lines when a key is pressed. IC4(b), C3 and R4 act as a monostable and the short pulse produced by IC4(b) is used for strobing the SELECT line of the RAM, in programming mode, to cause the data on the bus to be latched. As the strobe pulse occurs on the falling edge of the SID output of IC2 the data is sure to be stable on the bus. The rising edge of this pulse, after inversion by IC4(e), increments the RAM address on IC9, ready for the next number to be stored. During validation the $\overline{CS}$ line of the RAM does not need to be strobed and so the line is held permanently low when the PROG line goes high, via IC4(f) and IC7a. IC5(a) is used to latch the output of the comparator just as the key is released, this prevents an incorrect reset pulse being produced by IC3 when the RAM address is incremented and the input from the user is being waited for.

The four bit output on the user port can now be decoded as required. If ten separate control lines are required (for example 0-9) then this can be done simply by connecting a 74LS164 on the output bus and using the VALID line to control its ENABLE input. It is important to remember that the '0' button actually produces the number ten at the output (1010 in binary), not a zero. The display suggested in figures (1) and (2) is provided using the circuit in Fig 5), though because of the point just mentioned the output will not be meaningful when zero is entered, nor '*' and '#'.

Fig. 5. Display decoding.



Components

Resistors

R1	3.3kΩ
R2	330kΩ
R3	270kΩ
R4	1MΩ
R5	1MΩ
RSIL1	10 SIL resistor array

Capacitors

C1	0.1µF
C2	0.1µF
C3	0.1µF
C4	100µF Electrolytic
C5	10µF Electrolytic
C6	0.1µF
C7	10µF Electrolytic
C8	0.1µF

Semiconductors

IC1	4063 – 4-bit comparator
IC2	MV8870-1 – DTMF decoder
IC3	4063 – 40-bit comparator
IC4	74LS14 – Hex invertor
IC5	74LS74 – Dual D-type flip-flop
IC6	74LS244 – Tri-state buffer
IC7	74LS08 – Quad AND
IC8	2114 – Static RAM
IC9	74LS93 – 4-bit counter
IC10	74LS93 – 4-bit counter
IC11	7805 – +5V regulator

Miscellaneous

3.579545MHz NTSC Crystal
Cheap microphone or magnetic telephone pick-up
43 strips x 80 holes stripboard
Mains power adaptor delivering from 7V to 17V DC at at least 150mA

Construction

The circuit can be built on a piece of Veroboard of 43 strips width by 80 holes. Power supply decoupling capacitors should be provided for each chip of 0.1µF. The power supply into the regulator can be between 7V and 17VDC and if the answering machine used with the circuit has an external transformer, as most do, this should be able to power both this board and the answering machine (the board requires around 150mA current). The DTMF decoder is the only part not widely available. This was bought through ESD Electronic Services – Tel. (0279) 626777, part